Synchronous-Frame Harmonic Control for High-Performance AC Power Supplies

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***Abstract*—In order to achieve the reduction of voltage distortion in ac power supplies (ACPSs), this paper describes an implementation of synchronous-frame control for selected frequencies in the output voltage. The regulation of the fundamental output voltage, as well as that of some low-order harmonics, is achieved using a synchronous-frame controller for each selected frequency in addition to a conventional control. The conventional part conserves good dynamic performance under load changes, while rotating-frame controllers allow a slow, but very precise compensation of the residual errors within the assumption that the harmonics produced by distorting load are slowly varying. Moreover, motivated by a fixed-point implementation, a set of refinements and modifications of the original scheme is proposed, allowing a reduction of signal processing requirements and a new control algorithm structure less sensitive to quantization and rounding errors. This solution is particularly effective for high-power fully digitally controlled ACPSs, where the voltage loop bandwidth is usually not large enough to provide regulation at harmonic frequencies. The proposed control scheme has been implemented using a fixed-point single-chip digital signal processor (ADMC401 by Analog Devices). Experimental results on a 3-kVA three-phase converter prototype show the effectiveness of the proposed approach.**

***Index Terms*—Synchronous-frame control, uninterruptible power supplies, voltage control, voltage-source inverters.**

I. Introduction

THE limitation of voltage distortion in ac power supplies (ACPSs) or uninterruptible power supplies (UPS) feeding distorting loads is a challenging issue, which has stimulated the development of a variety of different control schemes [1]–[13]. This problem is particularly critical in those applications where, due to switching frequency limitation, the voltage loop bandwidth cannot be made large enough to compensate for harmonic frequencies, so that an expensive overrating of the output filter may be required in order to reduce the output voltage distortion.

In the attempt to overcome this problem, several high-performance feedback control schemes have been investigated, such as deadbeat control [9], [10], sliding-mode control [11], optimal state feedback [12], and many others [13]. Although these techniques are able to ensure very good results under large-signal disturbances, the total harmonic distortion (THD) on the output voltage due to nonlinear loads can be still quite high, especially in high-power applications.

Extensive research has also focused on different implementations of repetitive-based controllers [1]–[3], which are aimed to eliminate periodic disturbances, such as those deriving from diode and thyristor rectifiers. Under different degrees of approximation, they ensure high-quality sinusoidal voltage in spite of nonlinearities in the load. A different solution has also been proposed in [4], where selected harmonics are measured by a discrete Fourier transform (DFT) and compensated by integral controllers. As noted in [3], the scheme proposed in [4] does not allow unbalance compensation and its transient response is strongly limited by DFT filtering.

Following the reasoning of repetitive-based control schemes and extending the approaches proposed in [4] and in [16], this paper discusses the implementation of synchronous-frame control for some selected frequencies in the output voltage. Assuming that the load current harmonics are *slowly varying*, the regulation of the fundamental output voltage, as well as of some selected harmonics, is achieved using a rotating-frame controller [16], [20], [21] both for positive- and negative-sequence components of selected frequencies (for example, fundamental, 3rd, 5th, 7th, 9th, and 11th components) in addition to a conventional control, which ensures good dynamic performance under load changes. Moreover, motivated by a fixed-point implementation, a set of refinements and modifications of the original scheme is proposed, which allows a reduction of signal processing requirements by using equivalent stationary-frame regulation for the fundamental positive- and negative-sequence components [14], [15], [19]. To control voltage harmonics, instead, an innovative algorithm structure, which is directly related to repetitive-based solutions, is proposed, being less sensitive to quantization errors. Experimental results from a 3-kVA three-phase converter prototype using an Analog Devices fixed-point digital signal processor (DSP) (ADMC401) show the feasibility and effectiveness of the proposed approach.

II. Review of Synchronous-Frame Harmonic Control

The block diagram of the synchronous-frame control for the output stage of an ACPS is shown in Fig. 1, where the three-phase voltage-source inverter (VSI) is assumed to be without neutral wire; the forthcoming description, however, can be easily extended also for three-phase four-wire systems or for single-phase systems. Moreover, any possible different configuration of the VSI output filter can be included, such as the case where an insulating transformer is needed. Finally, a general block representing the rectifier input stage is also shown in Fig. 1. Focusing on the control of the output stage of

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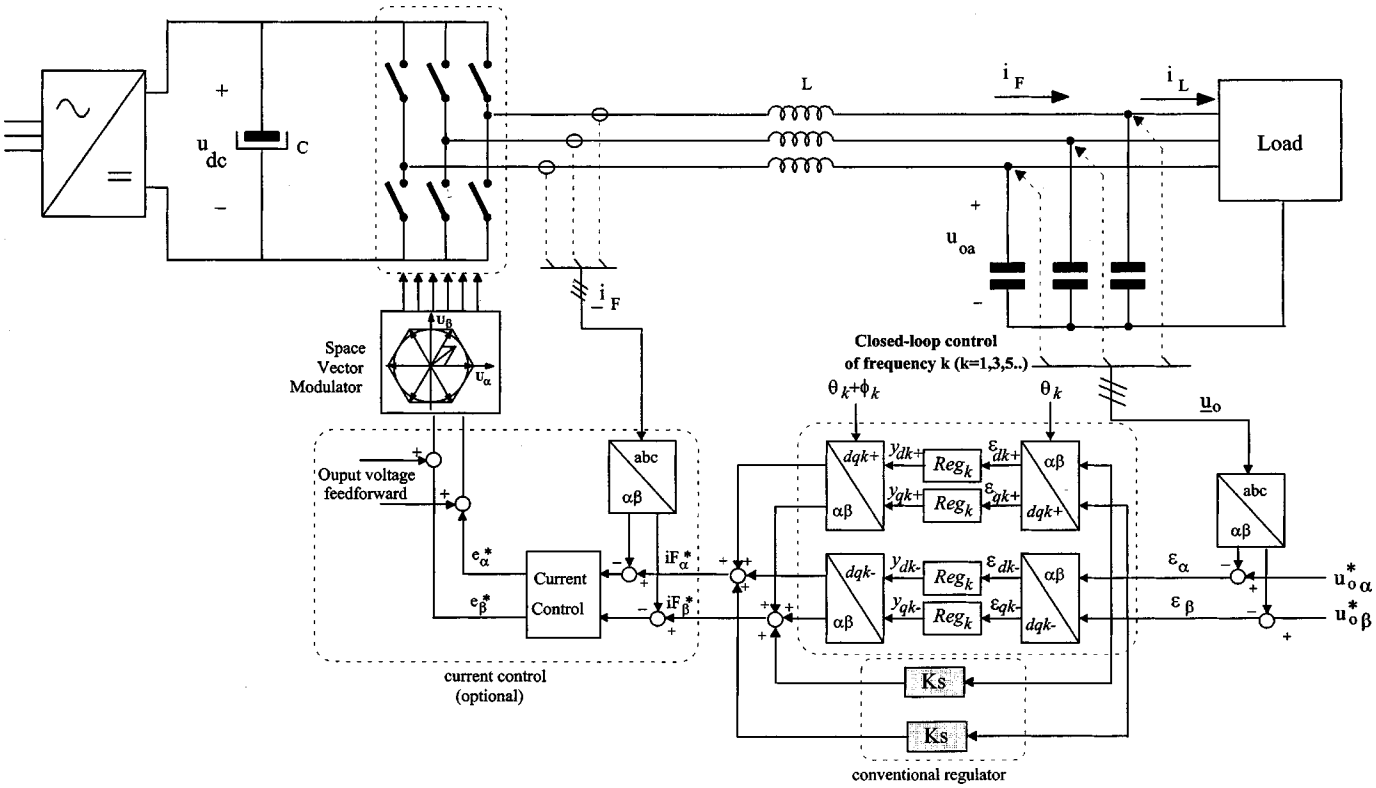

Fig. 1. General scheme for the voltage control of positive and negative components at selected frequencies.

an ACPS, the rectifier input stage is not discussed in this paper, but the effects of dc-bus variations on the proposed solution are described in Section VII.

Following the scheme of Figs. 1 and 2(a), output voltage errors $\vec{\varepsilon}_{\alpha\beta}$ $(\vec{\varepsilon}_{\alpha\beta} = \varepsilon_\alpha + j\varepsilon_\beta)$ in $(\alpha\beta)$ coordinates are first converted into synchronous reference frame quantities $\vec{\varepsilon}_{k+}$ $(\vec{\varepsilon}_{k+} = \varepsilon_{dk+} + j\varepsilon_{qk+})$, $\vec{\varepsilon}_{k-}$ $(\vec{\varepsilon}_{k-} = \varepsilon_{dk-} + j\varepsilon_{qk-})$ using both positive- $(dqk+)$ and negative-sequence transformations $(dqk-)$ rotating at angular frequency $\theta_k = k\omega_S$ (i.e., $\vec{\varepsilon}_{k+} = e^{j\theta_k}\vec{\varepsilon}_{\alpha\beta}, \vec{\varepsilon}_{k-} = e^{-j\theta_k}\vec{\varepsilon}_{\alpha\beta}$) where k is the order of the generic harmonic to be compensated and ω_S is the line angular frequency. All synchronous reference frame errors $(\varepsilon_{dk+}, \varepsilon_{qk+}, \varepsilon_{dk-}, \varepsilon_{qk-})$ are then compensated by regulators Reg_k, which ensure zero steady-state errors for each positive- and negative-sequence harmonic component. Of course, any possible homopolar term coming from the connection of the load neutral wire to the star point of the output filter capacitors cannot be compensated by the VSI in the configuration shown in Fig. 1. Then, the output of each regulator $(y_{dk+}, y_{qk+}, y_{dk-}, y_{qk-})$ is converted back to the stationary reference frames and possibly adding a leading angle ϕ_k which compensates for the delay of the remaining process. The current references $(i^*_{F\alpha}, i^*_{F\beta})$, if an internal current control is used, or the VSI voltage reference (e^*_α, e^*_β), if only a voltage control is the preferred choice (no VSI current sensing), are then obtained summing together the closed-loop regulations of the selected harmonics and the contribution given by the *conventional* stationary-frame controller K_s. Indeed, even if both solutions (with and without the internal current control) are possible, we focus on the former, which is advisable, in particular, for overcurrent protection.

The block diagram shown in Fig. 1 represents only a general solution which ensures compensation of the selected harmonics independently of any hypothesis on load symmetry. For specific loads, such as three-phase diode or thyristor rectifiers, simplifications could be adopted since, for example, the 5th harmonic has only negative-sequence components and the 7th harmonic has only positive components. Moreover, both harmonics derive from the 6th harmonic in the dq fundamental reference frame, so that only one regulator could be used for both harmonics. Given the generally unpredictable behavior of UPS loads, such assumptions are not considered here.

Even for the generic case, some simplifications of the theoretical scheme of Figs. 1 and 2(a) are possible [16]. First, it is easy to verify that the compensation of both positive- and negative-sequence harmonic components for a generic harmonic k is equivalent to the synchronous demodulation of the $\alpha\beta$ components, shown in Fig. 2(b), as long as all regulators Reg_k in Fig. 2(a) and (b) have the same transfer function. Secondly, even the scheme of Fig. 2(b) can be further simplified when implemented in DSPs since it is equivalent [14], [15] to the scheme of Fig. 2(c) with stationary-frame regulators $\mathrm{Reg}_{k\,\mathrm{AC}}$

$$\begin{aligned}\mathrm{Reg}_{k\,\mathrm{AC}}(s) &= \cos\phi_k[\mathrm{Reg}_k(s - jk\omega_s) + \mathrm{Reg}_k(s + jk\omega_s)] \\ &\quad + j\sin\phi_k[\mathrm{Reg}_k(s - jk\omega_s) - \mathrm{Reg}_k(s + jk\omega_s)]. \quad (1)\end{aligned}$$

III. Decomposition in Three-Layer Control Scheme

The general technique described in Section II is potentially able to eliminate any steady-state error for the selected frequencies. However, ACPS applications require specific dynamic per-

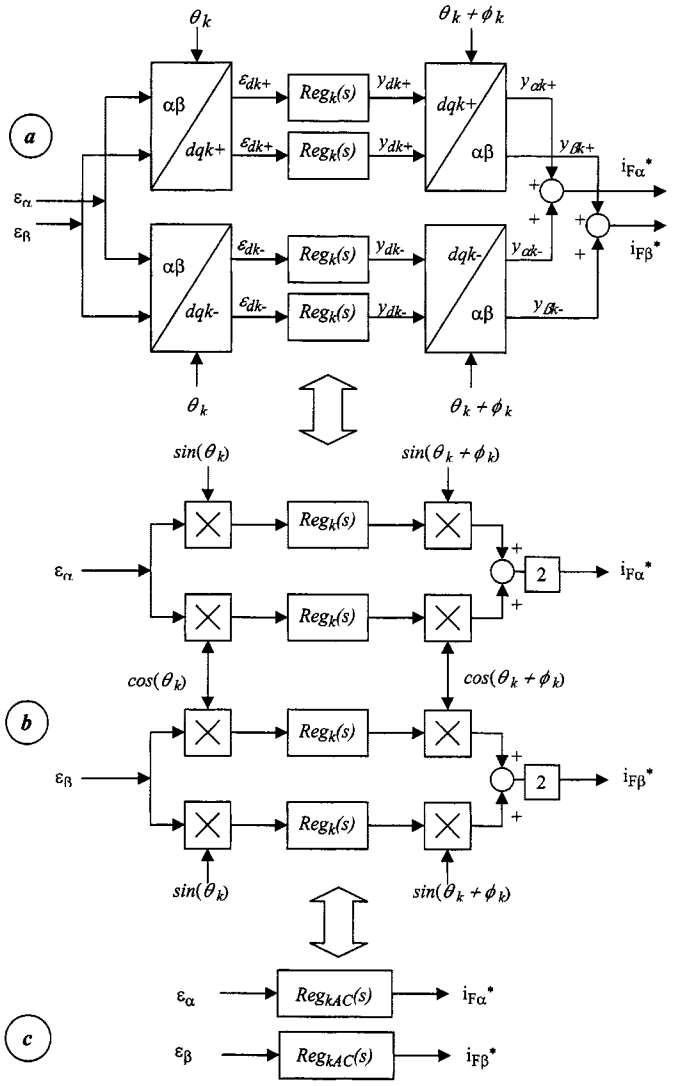

Fig. 2. Review of equivalency between stationary- and reference-frame controllers.

formance, so that we found useful to decompose the theoretical structure of Figs. 1 and 2 in a three-layer scheme, as reported in Fig. 3. Indeed, requirements on dynamic performance usually call for a very fast transient response with limited overshoot under load step changes and a precise and possibly fast regulation of fundamental components. The regulation of the harmonic components, instead, can be performed in some fundamental cycles as long as the harmonics of the distorting load are slowly varying. Indeed, this kind of time-scale decomposition in the output voltage regulation seems to be a mandatory choice in ACPS applications, since a short settling time also for the harmonic components causes a crosscoupling between different controllers, strongly reducing voltage regulation performance, especially in terms of overshoot limitation.

Motivated by this reasoning, the three-layer control scheme depicted in Fig. 3 is proposed. First, the proportional term K_P ensures a high speed of response under load changes. Second, the rotating-frame controllers for the fundamental components have been separated from the regulation of the harmonics components, being characterized by different speed of response.

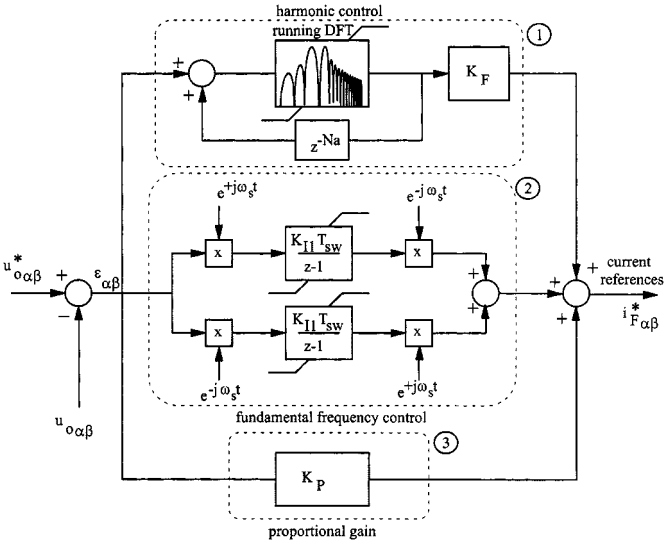

Fig. 3. Three-layer decomposition of the proposed voltage controller.

Aiming to reduce steady-state errors, a simple and effective choice for rotating-frame controllers is a pure integrator both for the positive- and the negative-sequence components

$$\mathrm{Reg}_k(s) = \frac{K_{Ik}}{s}. \tag{2}$$

This choice allows a direct design of parameters K_{Ik}, simply specifying the desired response time of harmonic components. Moreover, using transformation (1), regulators Reg_k given in (2) can be equivalently expressed in the stationary reference frame as

$$\mathrm{Reg}_{k\,\mathrm{AC}}(s) = 2K_{Ik}\left(\frac{s\cos(\phi_k) - k\omega_s\sin(\phi_k)}{s^2 + (k\omega_s)^2}\right) \tag{3}$$

which represents a *simple second-order passband filter* [14], [15], [19] with zero damping centered at the specified frequency. It is worth noting that we did not find it useful to introduce finite dc gain in (2) or, equivalently, any damping in (3), even in the presence of quantization and rounding errors due to fixed-point implementation, since the closed-loop poles are not dependent on the gain at the selected frequencies, but instead at the filter characteristics when the voltage open-loop gain crosses the 0-dB axis. However, it was very important to introduce an *antiwindup protection* algorithm, which was easily implemented saturating the output of the second-order filter (and, thus, also its internal state variable) to the maximum value foreseen at the design stage.

As an example, let us consider the compensation of the fundamental, 3rd, 5th, 7th, 9th, 11th, and 13th components using (2) for each rotating-frame controller (both for positive-sequence and negative-sequence components). Fig. 4 reports the open-loop gain of the resultant three-layer control scheme, where the proportional gain K_P has been set for a bandwidth of 250 Hz, the desired settling time is equal to 1/4 of the fundamental period for the fundamental components and to ten fundamental periods for the selected harmonics, while the leading time has been set equal to two modulation periods, partially compensating the delay of the current control. First, note in Fig. 4 that the high speed of response for fundamental components results in a wider bandpass filter, which increases

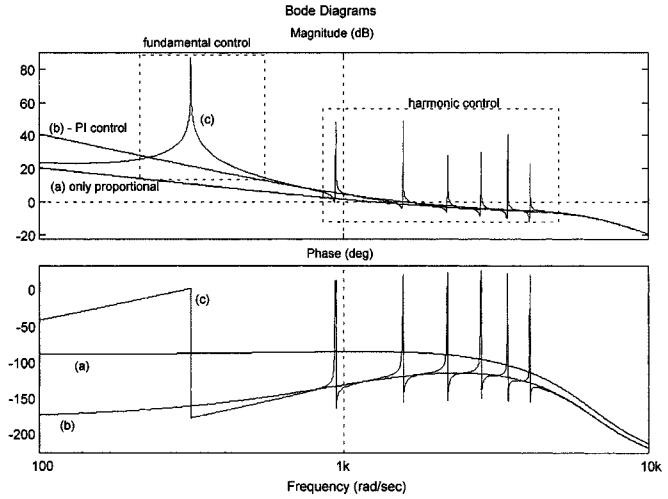

Fig. 4. Bode diagrams of the open-loop gain of *(a)* only P control, *(b)* conventional PI control, and *(c)* proposed control scheme.

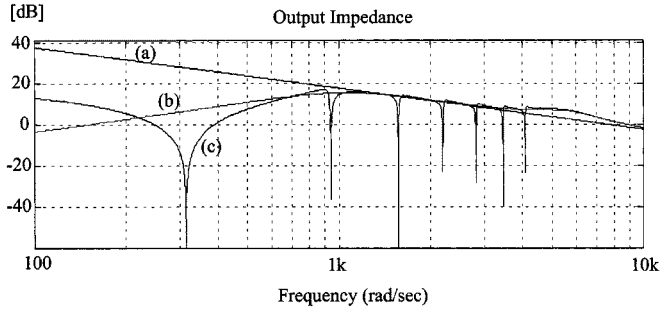

Fig. 5. *(a)* Impedance of the output filter capacitor, *(b)* closed-loop output impedance with a PI control, and *(c)* with the proposed solution.

the loop gain also around the fundamental frequency. Second, the diagram of Fig. 4 shows that the described harmonic control represents more a theoretical control algorithm than a practical one for fixed-point implementation, since the compensation of harmonic components requires the implementation of very narrow passband filters, which we found difficult on a fixed-point 16-bit DSP, unless 32-bit operation is considered at the expense of unacceptable complexity.

IV. A Solution for Fixed-Point Implementation

In order to solve the aforementioned drawbacks on the harmonic control, a set of refinements and approximations is investigated. For the purpose of explanation, let us consider the case of leading angle ϕ_k equal to zero. First, note that the desired transfer function for the harmonic control can be written as

$$\mathrm{Reg}_{h\,\mathrm{AC}}(s) = \sum_{h\in N_h} \frac{2K_{Ih}s}{s^2+(h\omega_s)^2} = K_F \sum_{h\in N_h} \frac{F_h}{1-F_h} \quad (4)$$

where

$$F_h(s) = \frac{2\xi_h h\omega_s s}{s^2+2\xi_h h\omega_s s+(h\omega_s)^2} \quad K_F = \frac{K_{Ih}}{\xi_h h\omega_s} \quad (5)$$

ξ_h being the arbitrary damping factors for passband filter F_h, and N_h the set of selected harmonic frequencies. From (4), we observe that the each of the original bandpass filters can be seen as a unity positive feedback of a bandpass filter F_h having unity gain and zero phase at the selected frequency h. Following this straightforward consideration and taking into account that $\xi_h$can be chosen as small as desired, (4) could be further approximated—only for all frequencies around the selected frequencies—by the following expression:

$$\begin{aligned}\mathrm{Reg}_{h\,\mathrm{AC}}(s) &= K_F \sum_{h\in N_h} \frac{F_h}{1-F_h} \\ &\approx K_F \frac{\sum_{h\in N_h} F_h}{1-\sum_{h\in N_h} F_h} \end{aligned} \quad (6)$$

as long as all passband filters are very selective (i.e., $F_{h1} * F_{h2} \ll F_{h1}, F_{h2}$). This is particularly true if we consider the moving or running DFT filters [17], [18] with a window equal to one fundamental period, such as

$$F_{dh}(z) = \frac{2}{N}\sum_{i=0}^{N-1} \cos\left[\frac{2\pi}{N}hi\right] z^{-i} \quad (7)$$

which realize zero gain at the nonselected frequencies. Indeed, (7) can be seen as a finite-impulse response (FIR) passband filter of N taps (N being the number of samples within one fundamental period) with unity gain and zero phase at harmonic h. One of the major advantages of (7) and approximation (6) is that the compensation of more harmonics does not add any increase in the computational complexity since

$$\sum_{h\in N_h} F_{dh}(z) = \frac{2}{N}\sum_{i=0}^{N-1}\left(\sum_{h\in N_k} \cos\left[\frac{2\pi}{N}hi\right]\right) z^{-i}. \quad (8)$$

Thus, only a change in the coefficients of the FIR filter is needed for the compensation of more harmonics without any additional calculations. As a result, only a positive feedback of (7) is needed to perform an approximated frequency response of the harmonic control regulator $\mathrm{Reg}_{h\,\mathrm{AC}}$.

This reasoning can be easily extended introducing also the leading angle ϕ_h as long as it is assumed proportional to the harmonic order h, or, in other words, as long as the leading time is assumed constant for all harmonics. The results, not reported here, show that a leading of N_a sampling intervals, N_a times the sampling period being the desired leading time, is introduced in (8) as follows:

$$\sum_{h\in N_h} F_{dh}(z) = \frac{2}{N}\sum_{i=0}^{N-1}\left(\sum_{k\in N_k} \cos\left[\frac{2\pi}{N}k(i+N_a)\right]\right) z^{-i}. \quad (9)$$

Then, a delay of N_a steps is needed in the feedback path to recover zero phase shift of the loop gain at the desired frequencies. This is, indeed, the situation depicted in Fig. 3, where a positive feedback of (9) is performed using a delay block z^{-N_a}. Indeed, we found this solution much less sensitive to quantization and rounding errors for fixed-point implementation with respect to that described in Section III. It is worth noting that the proposed solution is related to repetitive-based control schemes [1]–[4]. However, as compared to [1]–[4], we are able both to perform selective control on some harmonic voltages and to adjust the leading phase to ensure a proper stability margin.

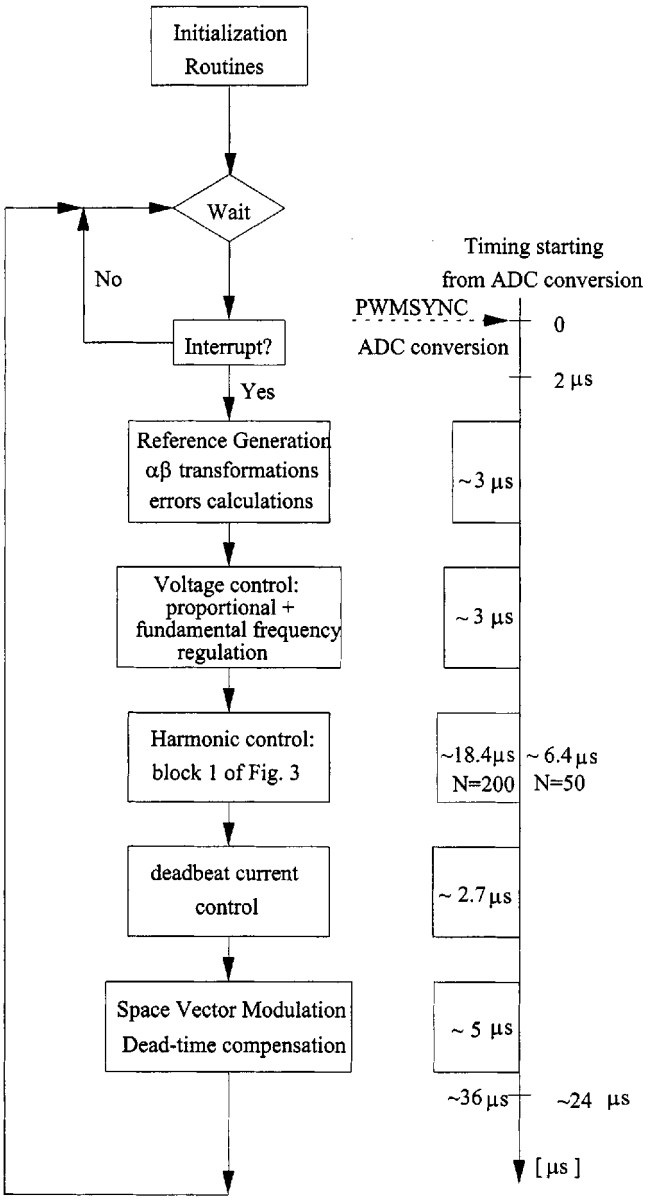

Fig. 6. Flowchart of the implemented control algorithm on ADMC401.

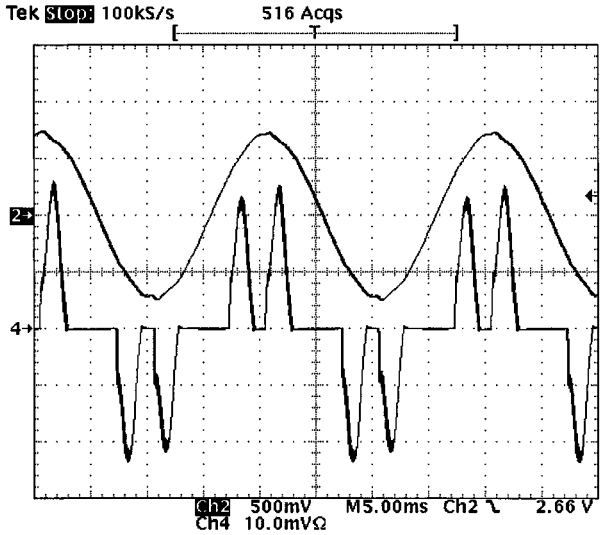

Fig. 7. Three-phase rectifier load with the proposed solution (output voltage, 100 V/div; output current, 10 A/div).

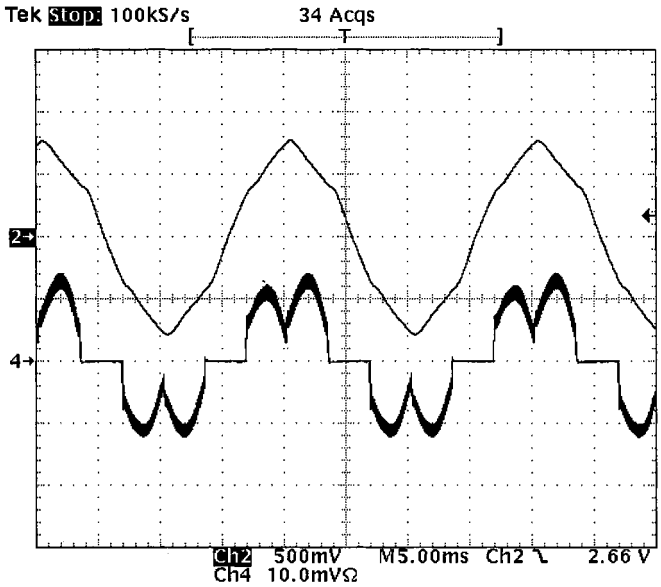

Fig. 8. Three-phase rectifier load with conventional PI control (output voltage, 100 V/div; output current, 0 A/div).

V. Design Criteria

Control parameter selection can be performed using the following procedure. First, the proportional gain can be chosen equal to that obtained from a conventional proportional plus integral (PI) design, given the specifications in terms of voltage loop bandwidth ω_c and phase margin m_ϕ. Second, selecting $\phi_1 = 0$, the integral gain K_{I1} can be set so as to ensure the same voltage loop bandwidth ω_c and phase margin m_ϕ of the conventional PI control, i.e.,

$$K_{I1} = K_{Ic}\frac{\omega_c^2 - \omega_s^2}{2\omega_c^2} \tag{10}$$

where K_{Ic} is the integral gain of the conventional PI control. Third, parameter N_a is aimed toward the compensation of the delay of the current control loop and typical values are in the range between 2–4, depending on the current control implementation. Finally, parameter K_F is set depending on desired speed of response for the harmonic component. Under the assumption of very narrow bandpass filters, parameters K_{Ik} can be chosen as

$$K_{Ik} = \frac{2.2}{n_{pk}T_S M_k} \tag{11}$$

where $(n_{pk}T_S)$ is desired response time (evaluated between 10% and 90% of a step response) for the generic harmonic k, n_{pk} is number of fundamental periods T_S, and M_k the module of the transfer function seen by the harmonic controller (including blocks 2 and 3 of Fig. 3). Then, following the approximation of Section IV and using the same integral term K_{IK} for all harmonics, we found out that K_F can be approximated by

$$K_F \approx \frac{K_{Ik}}{0.32\omega_s}. \tag{12}$$

After this preliminary design, a stability analysis is needed in order to verify that the overall closed-loop system has a proper phase margin, especially at harmonic frequencies. As an example, following the parameters used for Fig. 4, the closed-loop output impedance obtained using the described procedure is reported in Fig. 5. As foreseen, a strong attenuation is obtained at the selected frequencies, while outside those frequencies the behavior is similar to that obtained with a PI control.

Regarding the type of load applications of the proposed solution, it is worth noting that our algorithm seems to be particularly efficient with distorting loads, since its main goal is the reduction of voltage distortion. Moreover, it also gives some benefits with linear ohmic and inductive load, mainly for the regulation of the fundamental frequency and the THD reduction caused by deadtimes. However, we have also noted that it is also much more sensitive to parameter variations compared to PI control with capacitive or resonant loads. Thus, it seems to be less suited when the load is made by capacitors whose rating is closed to nominal output power.

VI. DSP Implementation

The proposed control strategy has been practically implemented by means of the 16-bit fixed-point DSP-based controller ADMC401. This DSP unit represents a powerful tool for digital control implementations for high-performance motion control industrial applications due to the fast arithmetic unit (38.5-ns cycle, 26 MIPS) and several memory-mapped peripherals and embedded memories, which make it suited for single-chip solutions. In fact, besides 1-kbyte RAM for data memory, 2-kbyte RAM for program memory, and 2-kbyte ROM program memory for boot load routines and debug features, it includes all the necessary facilities for implementing voltage and current control loops in a three-phase VSI, such as a high-resolution pulsewidth modulation (PWM) modulator, flash 12-bit A/D converters, which allow conversions up to eight channels in less than 2 μs, event capture channels, etc.

The flowchart and the timing of the implemented algorithm are represented in Fig. 6. Besides some initialization routines, control algorithms are evaluated within a service routine started by the interrupt generated at the end of the A/D conversion process, which is triggered by the PWMSYNC signal of the PWM modulator. As shown in Fig. 6, the major routines are related to the proportional and fundamental frequency bandpass filters with antiwindup (3 μs), the deadbeat current control (2.7 μs), the space-vector modulation (SVM) and the deadtime compensation (5 μs), and the control on the output voltage harmonics, which requires almost 18.4 μs when the running DFT is performed using 200 samples, but only 6.4 μs when using 50 samples. Note, however, that the timing reported here derives from a *nonoptimized* assembly code, where modularity instead of performance has been the major driving force during code development. As can be seen, the control routine requires, on the whole, about 36 μs (down to 24 μs for DFT on 50 samples).

VII. Experimental Results

The system of Fig. 1 has been experimentally tested using the following parameters: dc-link voltage, 370 V; VSI filter inductor, 1.5 mH; output filter capacitor, 90 μF; switching frequency $(f_{\rm sw})$, 10 kHz; and selected frequencies: 1st, 3rd, 5th, 7th, 9th, and 11th. It is worth noting that, in order to ensure sinusoidal voltage, even in the presence of distorting load, some additional margin on the dc-link voltage, compared to the value needed for linear load, is preferable to cope with the drop voltage of harmonic components on the inductive filter. Moreover, dc-bus variations have been compensated by a feedforward action in the SVM so as to avoid any additional distortion, especially when testing conventional solutions. It is worth mentioning that this is not strictly needed with the proposed approach since the proposed algorithm is able to compensated any possible voltage distortion, even that coming from dc-link voltage variations.

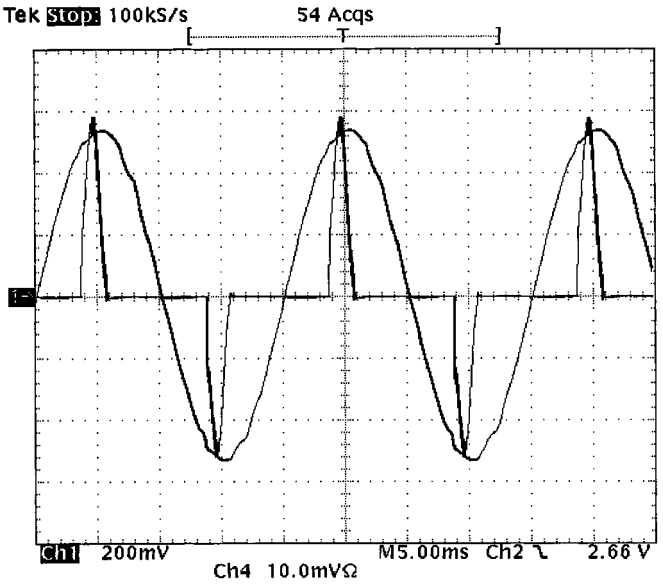

Fig. 9. Single-phase rectifier load with the proposed solution (phase-to-phase output voltage, 100 V/div; output current, 10 A/div).

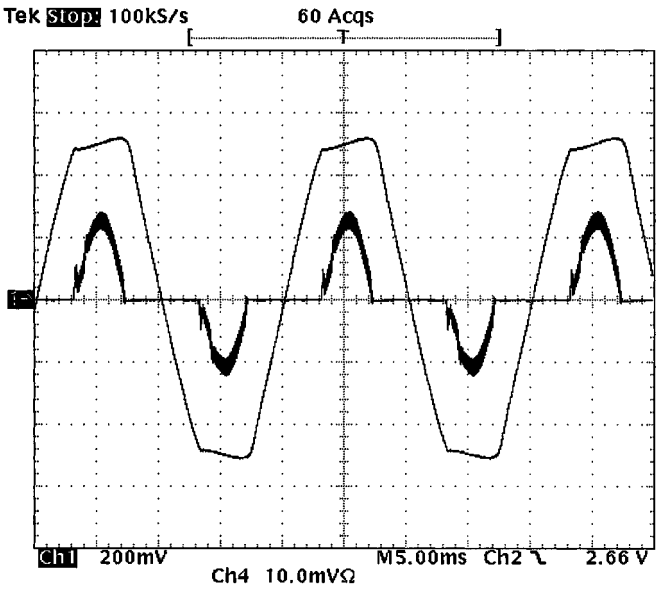

Fig. 10. Single-phase rectifier load with conventional PI control (output voltage, 100 V/div; output currentt, 10 A/div).

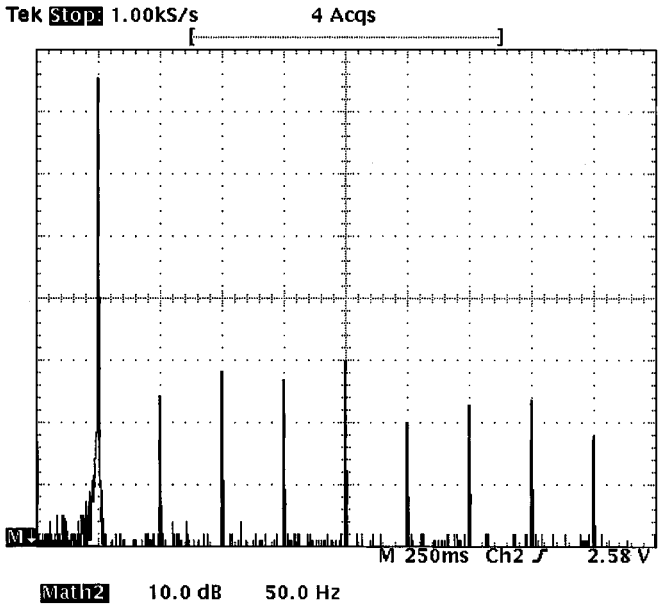

Fig. 11. Spectrum of output voltage with the proposed solution (vertical scale, 10 dB/div; horizontal scale, 50 Hz/div).

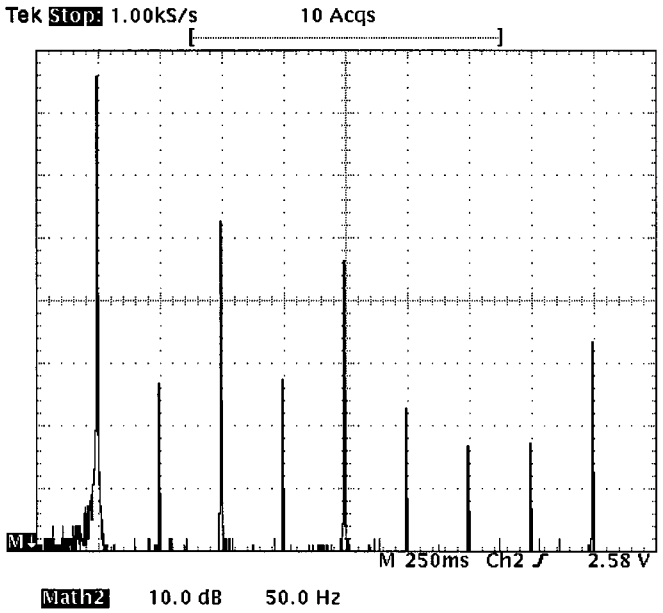

Fig. 12. Spectrum of output voltage with PI control (vertical scale, 10 db/div; horizontal scale, 50 Hz/div).

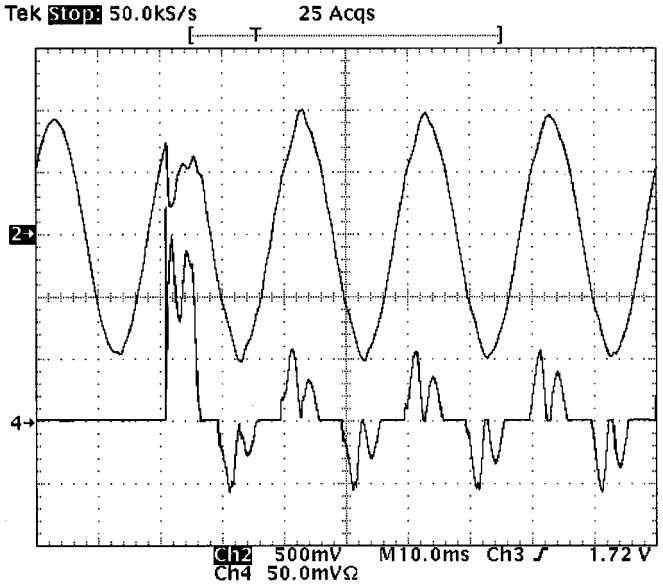

Fig. 13. Turn-on of a three-phase rectifier load with the proposed solution (output voltage, 100 V/div; output current, 20 A/div).

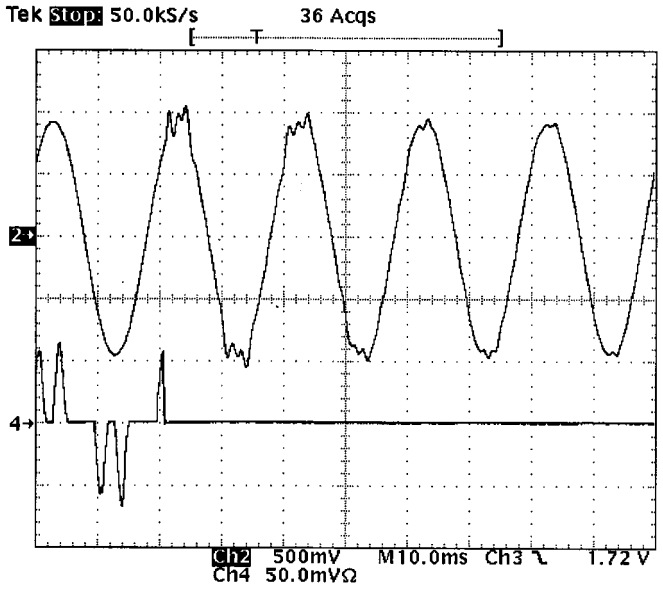

Fig. 14. Turn-off of a three-phase rectifier load with the proposed solution (output voltage, 100 V/div; output current, 20 A/div).

As far as the control parameters are concerned, the voltage loop bandwidth has been set to 400 Hz, phase margin equal to 50°, and 10 cycles for the harmonics components. For comparison, we have also implemented a conventional PI control, designed with the same bandwidth and the same phase margin.

The first investigation was performed with a three-phase diode rectifier with capacitive filter on the dc side. Fig. 7 reports the results obtained with the proposed solution, and Fig. 8 those obtained with conventional PI control. Note that the quality of the output voltage has been strongly improved, in spite of a great increase in load current harmonics arising from the reduced UPS output impedance.

In order to highlight the potentiality of the proposed system also during unbalance conditions, a single-phase diode rectifier has been applied between two phases. The results, reported in Figs. 9 and 10, clearly show the effectiveness of the harmonic voltage control. Moreover, Figs. 11 and 12 show the corresponding spectra of the output voltage, and we can note that all selected harmonics have been strongly reduced.

An investigation of the transient behavior under nonlinear load is reported in Fig. 13. Note that, besides an initial voltage drop due to switching to a discharged dc-link capacitor at the load side, the recovery of the output voltage to the nominal value is fast, while we observed that a complete correction of the output voltage distortion takes several fundamental periods.

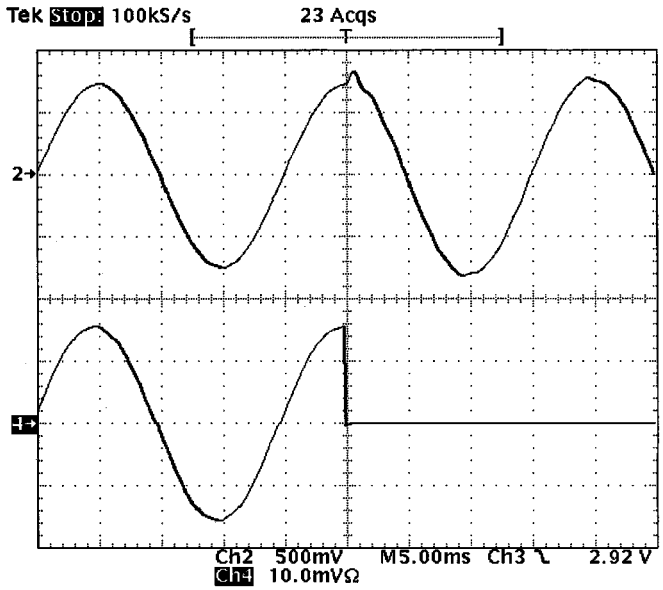

Fig. 15. Turn-off of a linear load with the proposed solution (output voltage and its reference, 100 V/div; output current, 5 A/div).

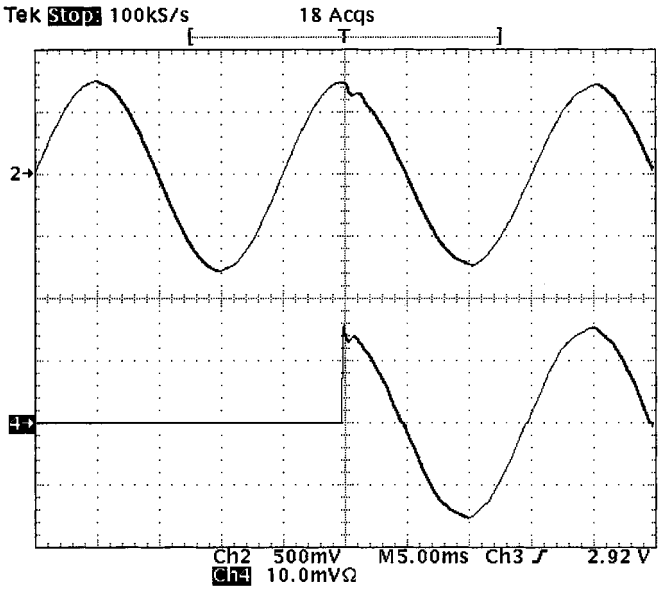

Fig. 16. Turn-on of a linear load with the proposed solution (output voltage and its reference, 100 V/div; output current, 5 A/div).

Indeed, we have experimentally tested that such harmonic correction takes around 8–10 periods, as predicted by our analysis, for distorting loads with inductive filters at the dc side, while it is longer with distorting loads with capacitive filters, such as those used in Fig. 13. This unforeseen behavior can be justified by the interaction between the UPS control and the dynamic component of the load, which, in the case of Fig. 13, increases the current harmonics as long as the UPS control reduces output voltage distortion, making the response time very difficult to predict. Finally, Fig. 14 reports the turn-off of a distorting load. It is worth noting that the ringing on the output voltage is mainly due to the integrators' dynamics on different harmonic reference frames, which takes some cycles to settle down. In this case, where we do have to take into account the dynamic component of the load, we have noted that the settling time for the harmonic components is around 6–7 cycles. This behavior is an inherent disadvantage of the proposed techniques.

Finally, transients with linear loads are also investigated. Fig. 15 shows the results with step-load turn-off and Fig. 16 for the step-load turn-on at reduced power level. Note that, in both cases, the transient behavior is excellent and we have verified, under separate tests not reported here, that overshoots and undershoots under step changes have not been increased with respect to those obtained with conventional PI control under the same transient conditions.

VIII. Conclusion

This paper has described how the reduction of voltage distortion caused by *slowly varying* harmonic currents can be obtained by using synchronous-frame harmonic regulators for the fundamental and some selected harmonic components, both for positive- and negative-sequence components. A set of refinements of the theoretical scheme, which better fit to fixed-point implementation, is proposed, allowing a reduction of signal processing requirements and leading to an innovative algorithm structure for the harmonic control, less sensitive to quantization and rounding errors. The proposed control scheme has been implemented using a fixed-point single-chip DSP ADMC401 by Analog Devices. Experimental results on a 3-kVA three-phase converter prototype show the feasibility, effectiveness, and advantages of the proposed approach.

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